REMARKS

The Final Action dated October 20, 2005 in this Application has been carefully considered. Claims 1-20 are pending. The following remarks are presented in a sincere attempt to place this Application in condition for allowance. Reconsideration and allowance are respectfully requested in light of the following remarks.

Applicants wish to thank the Examiner for the courtesy of the interview conducted on December 20, 2005. During the interview, the following remarks were discussed.

As a preliminary matter, Applicants respectfully traverse the Examiner's characterization of Applicants' previous Response. Specifically, the Examiner stated that "Applicant's arguments are deemed moot in view of the following new ground of rejection as explained here below, necessitated by Applicant['s] substantial amendment (i.e., a method wherein fixed snoop response time for source-clocked multiprocessor busses) to the claims which significantly affected the scope thereof." Final Action, Page 2. Applicant's Response (of July 21, 2005) made one change to Claim 10 and added Claims 19 and 20. However, in light of the following remarks, Applicants respectfully traverse the Examiner's characterization and respectfully submit that the current Claims are in condition for allowance.

Claims 1-20 stand rejected under 35 U.S.C. §103(a) by U.S. Patent No. 5,555,382 by Thaller et al. ("Thaller") in view of U.S. Patent No. 5,555,382 by Kato et al. ("Kato"), further in view of U.S. Patent No. 6,754,838 B2 by Burns et al. ("Burns"). Insofar as they may be applied against the Claims, these rejections are traversed and overcome.

Regarding Claim 1, Thaller was cited as assertedly fully disclosing the following:

(1) "a first microprocessor having one or more interfacing logics including a first interfacing logic, the first microprocessor being clocked by a first system clock (*fig. 2, items 14, 202, 226, 234-236, 260; column 7, lines 27-53*)" (Final Action at 3); and

(2) "a memory controller connected to the first interfacing logic through at least a first bus for transmitting at least a first signal from the memory controller to the first interfacing logic, the memory controller being clocked by a second system clock (*fig. 2 items 18, 106, 114-116; column 6, lines 27-57*)" (Final Action at 3).

The Examiner admits that Thaller does not teach in detail "a second microprocessor connected to the memory controller through at least a second bus for transmitting at least a second signal from the memory controller to the second processor, the second bus requiring a first period of time more to transmit the second signal than what the first bus requires to transmit the first signal, the first interfacing logic delaying the first signal by the first period of time so that the first and the second signals are respectively received by the first and the second microprocessors substantially at the same time." Final Action at 4.

The Examiner proposes two references to supply the Claim elements admittedly missing in Thaller. First, the Examiner cites Kato as allegedly fully disclosing:

(1) ". . .the processor system comprises first and second buses and a plurality of bus masters including a CPU 1301, a Picture Processor 1302, a Sound Processor 1303 and a DMA (Direct Memory Access) controller 1304, all connected to both buses;"

(2) "a plurality of bus slaves including an internal memory 1304 [sic], and I/O control circuit 1308, a universal timer 1309, and A/D converter 1310 and an optional DRAM refresh 1315, all connected to the first bus;"

(3) "a first bus arbitrator 1306 and a second bus arbitrator 1307 provide the arbitration for the first and second bus respectively;"

(4) "the processor system also include a PLL (Phase Locked Loop) circuit 1311, a clock driver 1312, a low voltage detector 1313 and an external memory interface 1313[sic]. . ." Final Action at 4 (*citing* Kato, Fig. 8; col. 8, lines 61-67; col. 9, lines 1-25).

Second, the Examiner cites Burns as assertedly fully disclosing ". . .a system capable of transmitting data to a plurality of processors generating two clock signals, the length of which when traced differ by the amount of tuning etch required to add sufficient delay to the forwarded clock signals transmitted to the processors. . ." Final Action at 4-5 (*quoting* Burns, fig. 4, items 300, 100a-b, 8, 370, 390; column 6, lines 28-67; column 7, lines 1-44).

The Examiner further stated that it would have been obvious "to have incorporated Kato teachings a second microprocessor connected to the memory controller, with the clock signals of Burns generating the delay, with the teachings of Thaller, for the purpose of 'providing a transmission scheme that offers reliable data transfer between devices while minimizing latency and skew and maximize bandwidth' as stated by Burns in lines 12-19 of column 3." Final Action at 5. Additionally, the Examiner contends that Thaller provides a motivation to combine "by stating 'providing a bus arbiter that reduces idle time and avoids wastage of bus bandwidth' in lines 1-4 of column 5." Final Action at 5. Further, the Examiner contends that Kato also provides a motivation to combine "by stating that there is an option to provide optimization of bus utilization dynamically in lines 36-39, column 4." Final Action at 5. Applicants respectfully submit that the Examiner's proposed combination fails to disclose each and every element as recited in Claim 1.

In particular, there is no motivation in Thaller to combine the teachings of Burns or Kato, and, even if, arguendo, there was motivation to combine, the proposed combination does not

disclose each and every element of Claim 1. First, the Examiner's cited motivation in Thaller recites as an advantage of the Thaller invention, "[t]his feature of the [Thaller] invention, allows the processor to complete any ongoing cache access and to gracefully relinquish the cache, without the need for an elongated bus transaction. In this manner, idle time is reduced and wastage of bus bandwidth is avoided." Thaller, col. 4, lines 66-67; col. 5, lines 1-4. After describing several embodiments of the Thaller invention, Thaller summarizes, "[i]n the above manner, timing and synchronization problems which may result from command errors are avoided, without elongating all bus transactions to the same size as is done in known computer systems. Thus, the computer system 10 of the [Thaller] invention avoids the associated delay and wasted bus bandwidth that results from the elongation of bus transactions." Thaller, col. 57, lines 63-67; col. 58. lines 1-2.

Therefore, according to Thaller, the thrust of the system disclosed in Thaller is to selectively provide idle bus cycles on a system bus so that a processor has ample opportunity to access its shared local cache. That is, instead of elongating all bus transactions to the same size, Thaller introduces idle bus cycles. In one specific embodiment, Thaller "reduces the amount of wasted bus bandwidth and prevents the unnecessary delay associated with having to re-arbitrate for the system bus 28 by asserting a STALL signal *on the system bus* 28 as opposed to conducting a NULL transaction." Thaller, col. 54, lines 13-17 (emphasis added).

In the Thaller system, the bus interface unit *of the CPU module* asserts idle bus cycles (e.g., a STALL command) on *the entire system bus*. *See* Thaller, col. 53, lines 18-47. A bus arbiter introduces the idle bus cycles in Thaller. "[T]he primary CPU module's bus interface unit 232 receives request to access the system bus 28" and "has the capability of inserting one or more idle bus cycles, where each idle bus cycle comprises a bus clock cycle during which *no module* on the system bus 28 is granted access to the system bus 28." Thaller, col. 54, lines 49-50 and 58-61.

In contrast, in the present invention, the *receiving end* of a first bus signal on a first unidirectional point-to-point bus delays the first bus signal while a second bus signal on a second unidirectional point-to-point bus is transmitted to a *different* receiver. In Thaller, the bus arbiter introduces idle bus cycles, as described above. In the present invention, the bus transaction *destination* module delays a signal. As recited in Claim 1, for example, "the first interfacing logic [of the first microprocessor] delay[s] the first signal by the first period of time so that the first and the second signals are respectively received by the first and the second microprocessors substantially at the same time." The first signal is transmitted "from the memory controller to the first interfacing logic," as recited in Claim 1. Clearly, Thaller does not teach, disclose, or suggest the destination module of a bus transaction delaying a signal.

Thus, it is clear that Thaller does not teach the claimed limitations as recited in Claim 1, as the Examiner admits, as described above. Neither does the Examiner's proposed combination with Burns or Kato supply the missing elements. In particular, neither Thaller nor Burns nor Kato teach "*the first interfacing logic delaying the first signal* by the first period of time so that the first and the second signals are respectively received by the first and the second microprocessors substantially at the same time" with "a first microprocessor having one or more interfacing logics including a first interfacing logic" and "a memory controller connected to the first interfacing logic through at least a first bus for transmitting at least a first signal *from the memory controller to the first interfacing logic*," as recited by Claim 1 (emphasis added).

Instead, Burns discloses "delay in the forwarded clock signal is generated *at the transmitting device* by adding tuning etch," (Burns, Abstract, emphasis added) with "the major advantage of [the Burns] technique is that it *eliminates the need to insert tuning etch upstream* to the forwarded clock signal associated with each individual data bundle." Burns, col. 7, lines 6-8 (emphasis added). Not

only does Burns not disclose the same method or system for delaying a signal as the present invention, Burns teaches generating a delay *at the transmitting device*, affirmatively teaching away from the present invention. As described above, Claim 1 recites "the first interfacing logic delaying the first signal," where the first microprocessor includes the first interfacing logic and the first bus transmits "at least a first signal from the memory controller to the first interfacing logic." Thus, for at least this reason, the proposed combination of Thaller and Burns does not disclose each and every element of Claim 1.

But the Examiner also offers Kato as disclosing, "a second microprocessor connected to the memory controller, with the clock signals of Burns generating the delay." Final Action at 5. As described above, Burns fails to disclose, teach, or suggest "the first interfacing logic delaying the first signal." Thus, even if, arguendo, Kato does disclose "a second microprocessor connected to the memory controller," as the Examiner asserts, the proposed combination of Thaller-Burns-Kato still fails to teach "the first interfacing logic delaying the first signal," as recited in Claim 1.

And Kato does not supply this missing element. Instead, Kato shows a multiprocessor architecture with a plurality of buses, each bus having more than one bus master and capable of transmitting both addresses and data. *See* Kato, Fig. 8, cols. 8-9. Each bus master is also connected to each bus through a plurality of bus interfaces. *See* Kato, Fig. 8, cols. 8-9. The thrust of Kato is to attempt to eliminate wasted high-speed bus bandwidth by allowing each bus master to access any common bus without also having to pass through any other bus. *See* Kato, Abstract; Fig. 8, cols. 8-9. In particular, according to Kato, "At every bus cycle, one set of priority order information is selected continuously and cyclically" and "When more than one bus master requests the bus access at the same time, the bus arbitrator determines which bus master may access the bus according to selected priority information." Kato, Abstract. Thus, as Kato teaches a bus arbitration scheme that

conflicts with the bus arbitration scheme of Thaller, there is no motivation to combine Kato with Thaller. For at least this reason, the Examiner's proposed combination fails to teach each and every element of Claim 1.

Further, nowhere does Kato teach, "the first interfacing logic delaying the first signal," as recited by Claim 1, where the first interfacing logic is the *destination* of a first signal sent "from the memory controller to the first interfacing logic." Instead, according to Kato, "The architecture of [the Kato] invention prevents the overall performance of a processor system from deterioration due to slower bus slaves." Kato, col. 3, lines 65-67. Thus, in contrast with the present invention, Kato attempts "to provide a high-speed processor system having *a bus arbitration mechanism* capable of optimizing bus utilization." Kato, col. 4, lines 1-3 (emphasis added). The focus in Kato is on a bus arbitration mechanism, not a delay mechanism "so that the first and the second signals are respectively received by the first and the second microprocessors substantially at the same time," as recited in Claim 1.

For at least this reason, Kato fails to provide each and every element admittedly missing in Thaller and proven absent in Burns. Thus, Applicants respectfully submit that the Examiner's proposed combination of Thaller-Kato-Burns fails to disclose each and every element as recited in Claim 1, and therefore Claim 1 is clearly and precisely distinguishable from these references and the remaining references of record. Accordingly, Applicants respectfully request that the rejection of Claim 1 under 35 U.S.C. § 103(a) be withdrawn and that Claim 1 be allowed.

The Examiner employed the same proposed combination and rationale in rejecting Claim 10 under 35 U.S.C. § 103(a). "The same motivation that was utilized in the combination of claim 1, applies equally as well to claim 10. By this rationale claim 10 is rejected." Final Action at 13. Applicants respectfully traverse this rejection and submit that the above reasoning overcoming the

Examiner's proposed combination with respect to Claim 1 is equally effective as applied with respect to Claim 10. In particular, nowhere does the Examiner's proposed combination of Thaller-Burns-Kato disclose, teach, or suggest, "the first interfacing logic delaying the first signal by the first period of time so that the first and the second signals are respectively received by the memory controller substantially at the same time," and "a first microprocessor connected to the first interfacing logic through at least a first bus for transmitting at least a first signal from the first microprocessor to the first interfacing logic," as recited by Claim 10. That is, as with Claim 1, the Examiner's proposed combination fails to teach the signal *destination* delaying the signal.

Therefore, for at least this reason, Claim 10 is clearly and precisely distinguishable over the cited references in a patentable sense. Accordingly, as the Examiner's proposed combination does not teach each and every element as recited in Claim 10, Claim 10 is therefore allowable over these references and the remaining references of record in any combination. Applicants respectfully request that the rejection of Claim 10 under 35 U.S.C. § 103(a) be withdrawn and that Claim 10 be allowed.

Claims 2-9 depend on and further limit Claim 1. Hence, for at least the aforementioned reasons, these Claims would be deemed to be in condition for allowance. Applicants respectfully request that the rejections of the dependent Claims 2-9 also be withdrawn. Similarly, Claims 11-18 depend on and further limit amended Claim 10. Hence, for at least the aforementioned reasons, these Claims would also be deemed to be in condition for allowance. Applicants respectfully request that the rejections of the dependent Claims 11-18 also be withdrawn.

Regarding Claim 19, the Examiner cited the proposed combination of Thaller-Kato-Burns as fully disclosing:

(1) "a first microprocessor comprising one or more interfacing logics including a first interfacing logic, the first microprocessor being clocked by a first system clock" (*citing* Thaller, Fig. 2, items 14, 202, 226, 234-236, 260; col. 7, lines 27-53);

(2) "a memory controller coupled to the first interfacing logic through at least a first high frequency, point-to-point, unidirectional, source-clocked bus for transmitting at least a first signal from the memory controller to the first interfacing logic, the memory controller being clocked by a second system clock" (*citing* Thaller, Fig. 2, items 18, 106, 114-116; col. 6, lines 27-57);

(3) "a second microprocessor comprising one or more interfacing logics including a second interfacing logic, the second microprocessor being clocked by a third system clock" (*citing* Kato, Fig. 8, col. 8, lines 61-67; col. 9, lines 1-25);

(4) "the second microprocessor coupled to the memory controller through at least a second high frequency, point-to-point, unidirectional, source-clocked bus for transmitting at least a second signal from the memory controller to the second interfacing logic, the second high frequency, point-to-point, unidirectional, source clocked bus requiring a first period of time more to transmit the second signal that what the first high frequency, point-to-point unidirectional, source-clocked bus requires to transmit the first signal" (*citing* Kato, Fig. 8, lines 61-67; col. 9, lines 1-25); and

(5) "wherein the first interfacing logic is configured to delay the first signal by a second period of time and the second interfacing logic is configured to delay the second signal by a third period of time so that the first signal and the second signal are respectively received by the first microprocessor and the second microprocessor substantially at the same time" (*citing* Burns, Fig. 4, items 300, 100a-b, 370, 390; col. 6, lines 28-67; col. 7, lines 1-44).

Applicants respectfully submit that the Examiner's proposed combination fails to teach each and every element as recited in Claim 19 for at least the same reasons that the Examiner's proposed

combination fails to teach each and every element as recited in Claims 1 and 10. In particular, as described above, Burns (and Thaller and Kato) fails to teach the *receiving* end of a bus transaction delaying a signal. Thus, the Examiner's proposed combination of Thaller-Burns-Kato fails to disclose, teach, or suggest, "wherein the first interfacing logic is configured to delay the first signal," as recited in Claim 19. For at least this reason, Claim 19 is clearly and precisely distinguishable over the cited references in a patentable sense, in any combination.

Moreover, there are a number of other elements clearly missing from the Examiner's proposed combination of Thaller-Burns-Kato. For example, the Examiner's proposed combination fails to teach, "the second microprocessor being clocked by a third system clock." Nor does the Examiner's proposed combination teach, "the memory controller being clocked by a second system clock." Likewise, the Examiner's proposed combination fails to disclose, delaying "the first signal by a second period of time," or delaying "the second signal by a third period of time so that the first signal and the second signal are respectively received by *the first microprocessor and the second microprocessor* substantially at the same time." (Emphasis added.)

Therefore, for at least these reasons, Claim 19 is clearly and precisely distinguishable over the cited references in a patentable sense. Accordingly, as the Examiner's proposed combination does not teach each and every element as recited in Claim 19, Claim 19 is therefore allowable over these references and the remaining references of record in any combination. Applicants respectfully request that the rejection of Claim 19 under 35 U.S.C. § 103(a) be withdrawn and that Claim 19 be allowed.

Claim 20 depends on and further limits Claim 19. Hence, for at least the aforementioned reasons, Claim 20 would be deemed to be in condition for allowance. Applicants therefore

respectfully request that the rejection of dependent Claim 20 be withdrawn and that Claim 20 also be allowed.

Applicants have now made an earnest attempt to place this Application in condition for allowance. For the foregoing reasons and for other reasons clearly apparent, Applicants respectfully request full allowance of Claims 1-20.

Applicants do not believe that any fees are due; however, in the event that any fees are due, the Commissioner is hereby authorized to charge any required fees due (other than issue fees), and to credit any overpayment made, in connection with the filing of this paper to Deposit Account No. 50-0605 of CARR LLP.

Should the Examiner deem that any further amendment is desirable to place this application in condition for allowance, the Examiner is invited to telephone the undersigned at the number listed below.

Respectfully submitted,

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